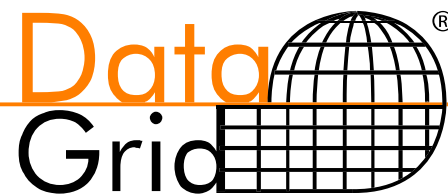


Lat: N 29 39 42.318

Lon: W 82 19 36.863



# **DGRX OEM L1/L2 GPS Receiver**

## **Technical Specification**

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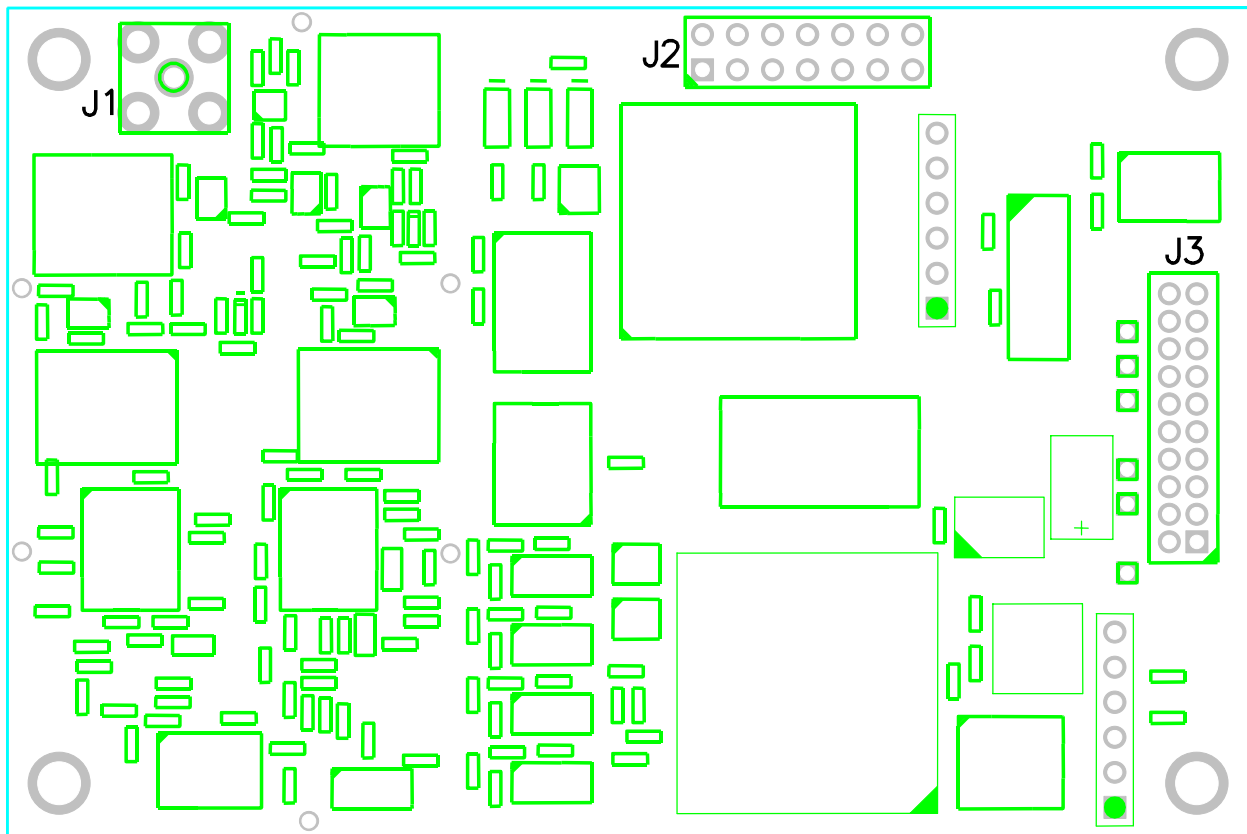
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## 1. General

The DGRx-GPS OEM receiver radio section has separate frequency paths for GPS L1 and GPS L2. A reconfigurable FPGA based section can allocate processing resources as needed. The default setting yields 28-channels, 14 GPS L1 and 14 GPS L2. Up to two channels can be dynamically reallocated for SBAS. Two asynchronous serial ports RS-232 are used to communicate with external devices.

General view of DGRx-GPS board is depicted in **Fig. 1**.



**Fig. 1. DGRx receiver board general view, shield removed.**

## 2. Input/output Interfaces

The DGRx-GPS receiver board has a single RF port J1 to connect an active GPS antenna and it has two input/output ports – J2 and J3.

J2 is a debugging connector and is not used in normal operation. J3 is intended for connection to the external equipment such as power supplies, host PCs or other equipment.

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## 2.1. RF Interface

The DGRx-GPS has a single RF port through which GPS L1 as well as L2 signals are fed using a single RF cable. The RF connector is an MCX straight female. DC antenna power can be supplied from the central conductor which is set positive. The potential supplied by the board is 3.3 Volt. Any other value below 25 Volt can be supplied using an external source by way of the J3 connector. Note that for both antenna power options, power is supplied without any protection circuitry on the board; hence any short in the antenna connection while the receiver is switched on may damage the board. However, if the short circuit current does not exceed 200mA, the receiver may be kept alive. **The external antenna voltage must be less than 25V DC.**

## 2.2. Output Interfaces

The debugging connector (J2 - pin strip header, two row, 2x7 pin, 0.1"x0.1") is not used in normal receiver operation and should not be mounted.

J3 is also pin strip header (two row, 2x10 pin, 2.0x2.0mm) and provides a connection to the external environment. The DGRx-GPS input/output signals (J3) are listed in *Table 1*.

Table 1

Pin	Name	Type (I/O)	Description
1	ANT_PWR	I	External antenna power, 25V DC max.
2	TXIA	O	Serial Port A transmit data (LVCMOS levels)
3	BAT	I	Backup battery, +2.0~3.6V DC
4	VDD	I	Main power, +3.3V $\pm$ 5%
5	MR	I	Manual reset, active low
6	PRG_FL	I	Programming flag, active low
10, 13, 16, 18	GND		Ground
8	RXIA	I	Serial Port A receive data (LVCMOS levels)
11	TXA	O	Serial Port A transmit data
12	RXA	I	Serial Port A receive data
14	TXB	O	Serial Port B transmit data
15	RXB	I	Serial Port B receive data
19	RXIB	I	Serial Port B receive data (LVCMOS levels)
20	TXIB	O	Serial Port B transmit data (LVCMOS levels)

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2, 7, 8, 9, 17			Not used
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## DGRx OEM Receiver Technical Specification

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### **ANT\_PWR**

External antenna power, maximum 25 Volt DC supply voltage.

### **BAT**

External backup battery voltage, +2.0~3.6V DC.

### **VDD**

Main power supply voltage, +3.3V  $\pm$ 5%.

### **MR**

Manual reset input, active low, 20K pull-up. Pulse width for manual reset should be at least 100ns.

### **PRG\_FL**

Programming flag input, active low, 20K pull-up. The DGRx-GPS firmware can be updated via the serial port.

### **TXA, TXB**

Transmit data ( $\pm$ 6V levels), Serial Port A and B, respectively.

### **RXA, RXB**

Receive data ( $\pm$ 6V levels), Serial Port A and B, respectively.

### **TXIA, TXIB**

Transmit data with LVCMOS (+3.3V) levels, Serial Port A and B, respectively.

### **RXIA, RXIB**

Receive data with LVCMOS (+3.3V) levels, Serial Port A and B, respectively.

**Note:** The RS-232 ports with LVCMOS levels can be connected to the receiver board only when the RS-232 transceiver IC is removed.

### 3. Back-up Mode

The receiver is switched to backup mode when the main board power (3.3V) is turned off and backup voltage is available on pin #3 of output connector J3. In backup mode, SRAM and RTC are connected to backup voltage. Therefore, in this mode the only devices that are retained in an active state are SRAM and RTC. Keeping these two devices in an active state, allows the handling of warm and hot starts. Satellite ephemeris data is kept in SRAM while the RTC provides an uninterrupted time and date count. Both devices can be kept alive with backup voltage down to 2.0V. The recommended backup voltage range is 2.0~3.6V.

### 4. Options

The receiver board can be configured in the following ways regarding the antenna supply voltage (“Antenna Power” Option).

The Antenna can be powered from two different sources: from internal 3.3V board power or from an external source.

#### 4.1. Using Internal 3.3V for powering the antenna.

To set the receiver to use the 3.3v internal source option, R2 (0 Ohm resistor) should be mounted and R1 (0 Ohm resistor) removed.

#### 4.2. Using External source for powering the antenna.

To set an external antenna power source, R1 should be mounted while R2 removed. In this case, the antenna supply voltage should be applied to pin #1 of the receiver output connector J3. *The external antenna power should not exceed 25V DC.*

## 5. Physical Properties

Size: 90 mm x 60 mm x 12 mm  
Weight: 32 g  
Power: 3.3 V, 1.5 W  
Operating temperature: -40°C to 85°C

Figure 2, 3 and 4 show the board outlines, connectors and mounting holes. All units are in inches.

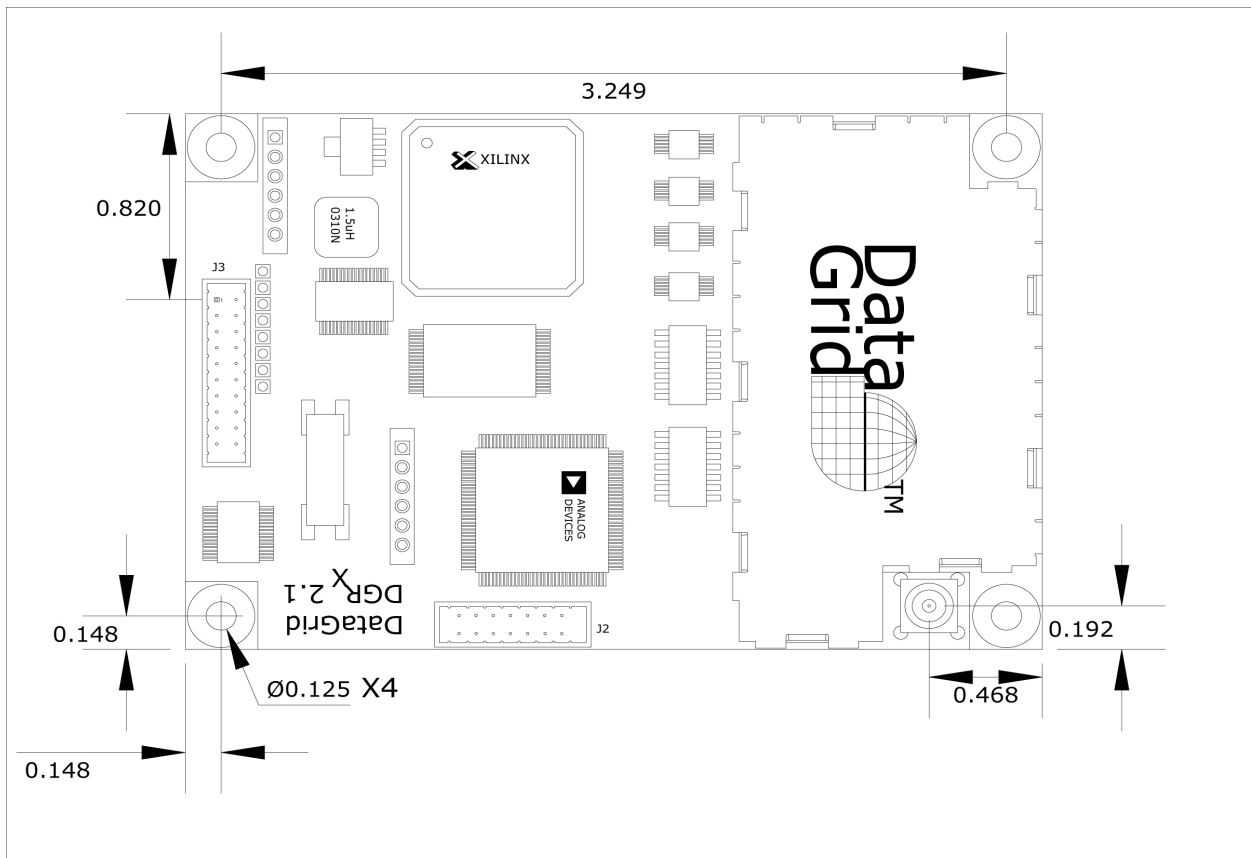
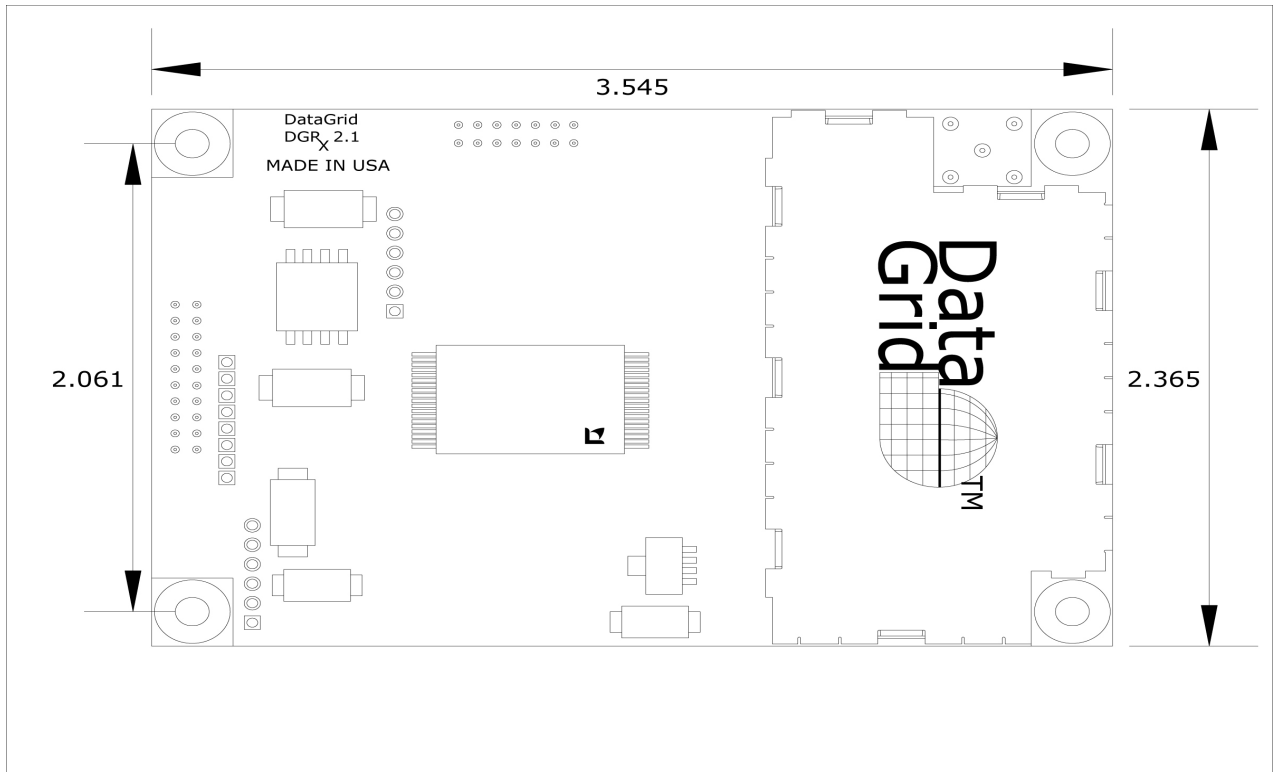
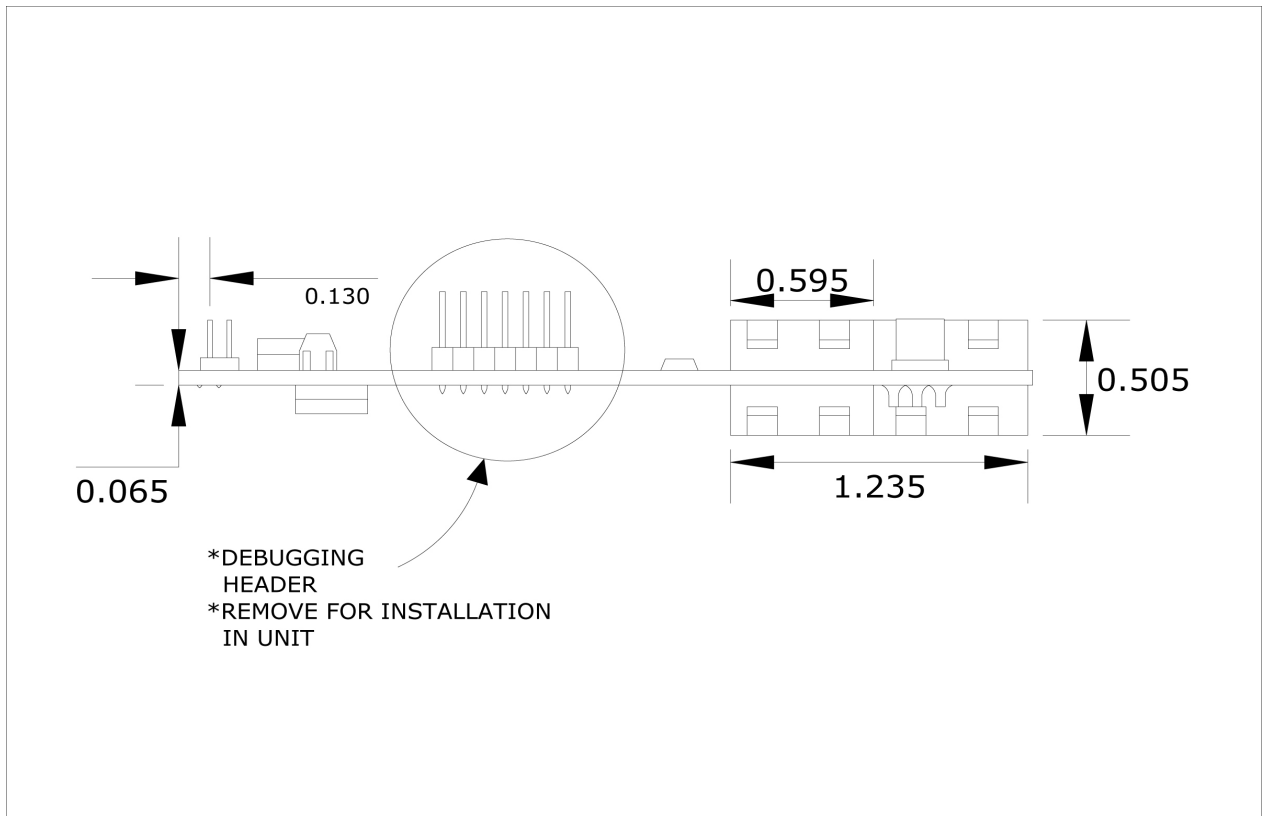


Fig. 2

# DGRx OEM Receiver Technical Specification



**Fig. 3**



**Fig. 4**